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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/675,420	09/30/2003	William H. Cochran	ROC920030199US1	6180

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EXAMINER	
SCHNEIDER, JOSHUA D	

ART UNIT	PAPER NUMBER
2182	

DATE MAILED: 02/28/2006

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/675,420	COCHRAN ET AL.	
	Examiner	Art Unit	
	Joshua D. Schneider	2182	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *30 September 2003*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-20* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-20* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

Claim Rejections - 35 USC § 112

1. The following is a quotation of the first paragraph of 35 U.S.C. 112:

> The specification shall contain a written description of the invention, and of the manner and process of making and using it, in such full, clear, concise, and exact terms as to enable any person skilled in the art to which it pertains, or with which it is most nearly connected, to make and use the same and shall set forth the best mode contemplated by the inventor of carrying out his invention.

2. Claims 1, 8, 15, and dependant claims 2-7, 9-14, and 16-20 are rejected under 35 U.S.C. 112, first paragraph, as failing to comply with the enablement requirement. The claim(s) contains subject matter which was not described in the specification in such a way as to enable one skilled in the art to which it pertains, or with which it is most nearly connected, to make and/or use the invention.

3. With regards to claims 1, 8, and 15, the system is not taught in such a way that all instances of the claimed set, integers, can be made or used by one of ordinary skill in the art. The claimed set of N instances of an element, where N is an integer is not taught for any negative instance, though such instances would seem to be unable to be made or used, they are encompassed by the current language of the claims.

4. The dependant claims 2-7, 9-14, and 16-20, are rejected for incorporating the non-enabled subject matter of the claims upon which they depend.

5. The following is a quotation of the second paragraph of 35 U.S.C. 112:

> The specification shall conclude with one or more claims particularly pointing out and distinctly claiming the subject matter which the applicant regards as his invention.

6. Claims 1, 8, 15, and dependant claims 2-7, 9-14, and 16-20 are rejected under 35 U.S.C. 112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which applicant regards as the invention.

7. With regards to claims 1, 8, and 15, the system is not described in such a way that all instances of the claimed set, integers, can be made or used by one of ordinary skill in the art. The claimed set of N instances of an element, where N is an integer is not taught for any negative instance, though such instances would seem to be unable to be made or used, they are encompassed by the current language of the claims. The limits of the scope of the claimed invention are therefore unclear.

8. With further regards to claim 15, it is also unclear what the difference is between an I/O line and spare I/O line. It would seem that any I/O line not being used at the current moment is spare for the purposes of a current transaction. For instance, any lines to a floppy disk drive not being used because the floppy drive is not being used is spare to the other operations ongoing in a standard computer. It is also not clear how such a spare I/O line could be connected to the limited inputs of the multiplexers of the dependant claims. Also it appears that the word "line" on line 16 of claim 15 should be "lines."

9. With regards to claims 7, 14, and 20, it is unclear how a multiplexer shifts signals on an I/O line to an adjacent multiplexer. This seems to be beyond the normal operation of a multiplexer, but the multiplexers are not described as being modified in any way. This would seem to allow the multiplexer to have additional output functions that cannot be found to exist in the basic multiplexer function. It may be that there is some sort of demultiplexing associated in a short feedback loop with the multiplexer, but this is not described or found in the claims or specification in a way that would allow one of ordinary skill in the art to make or use the invention.

10. The dependant claims 2-7, 9-14, and 16-20, are rejected for incorporating the non-enabled subject matter of the claims upon which they depend.

11. All further rejections and objections are made in view of the specification as best understood in light of the previous objections and rejections.

Claim Rejections - 35 USC § 102

12. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

13. Claims 1, 2, 4-9, 11-16, 19, and 20, are rejected under 35 U.S.C. 102(b) as being anticipated by U.S. Patent 5,909,594 to Ross et al.

14. With regards to claim 1, Ross teaches N I/O lines (Fig. 12, any data lines that input data from one point and output it to another), wherein N is an integer (selecting N to be 3), N internal networks (Fig. 12, elements 606-609 and there respective connections forming networks), N internal multiplexers for routing signals from individual I/O lines to individual internal networks in response to control signals (Fig. 12, elements 611-614, control signals for these multiplexers being inherent to the use of multiplexers), and a multiplex controller for producing said control signals (control signals inherent to the multiplexers must inherently be from some controller of the multiplexers, see column 17, line 40, through column 18, line 3).

15. With regards to claim 8, Ross teaches N I/O lines (Fig. 12, any data lines that input data from one point and output it to another), wherein N is an integer (selecting N to be 3), N addressable arrays (Fig. 12, elements 601-604), N multiplexers for routing signals from

individual I/O lines to said addressable arrays in response to control signals (Fig. 12, elements 611-614, control signals for these multiplexers being inherent to the use of multiplexers); and a multiplex controller for producing said control signals (control signals inherent to the multiplexers must inherently be from some controller of the multiplexers, see column 17, line 40, through column 18, line 3).

16. With regards to claim 15, Ross teaches a processor having at least W I/O lines (Fig. 13, element 703, and connection to element 702, at least 1 I/O line inherent to connection); a bus for transferring at least W I/O bits to and from said processor (Fig. 13, element 703, and connection to element 702, at least 1 I/O line inherent to connection), a memory module attached to said bus (Fig. 13, element 704, at least 1 I/O line inherent to connection), said memory module for storing and saving a W-bit wide word (Fig. 13, element 704, column 5, lines 44-56), wherein said W-bit wide word is applied to said bus (Fig. 13, element 704, column 5, lines 44-56, inherently must be applied in order to store in memory), wherein said memory module is comprised of a plurality of memory devices having more than W I/O lines, wherein at least one memory device has a spare I/O line that is not connected to said bus(connected to bus and controller), and wherein said at least one memory device (memory controller) includes: said spare I/O line (connection to packet switched router as discussed above); N-1 I/O lines (Fig. 12, any data lines that input data from one point and output it to another), wherein N is an integer (selecting N to be 3), N addressable arrays, at least one of which is associated with said spare I/O line (Fig. 12, elements 601-604); N multiplexers for routing signals from said N-1 I/O lines and from said spare I/O line to said addressable arrays in response to control signals (Fig. 12, elements 611-614, control signals for these multiplexers being inherent to the use of multiplexers); and a multiplex controller for

producing said control signals(control signals inherent to the multiplexers must inherently be from some controller of the multiplexers, see column 17, line 40, through column 18, line 3), wherein data on at least one of said N-1 I/O line can be stored in and/or read from said array associated with said spare I/O line (column 17, line 40, through column 18, line 3, from any other multiplexed line).

17. With regards to claims 2, 9, and 16, Ross teaches at least one multiplexer is an N-to-1 multiplexer (Fig. 12, elements 611-614, when N equals 3).

18. With regards to claims 4 and 11, Ross teaches at least one multiplexer is a 3-to-1 multiplexer (Fig. 12, elements 611-614).

19. With regards to claims 5 and 12, Ross teaches at least one multiplexer can route signals to and from N-1 multiplexers (column 17, line 40, through column 18, line 3, from any other multiplexed line).

20. With regards to claims 6, 13, and 19, Ross teaches each multiplexer can route signals to an associated array (column 17, line 40, through column 18, line 3, from any other multiplexed line).

21. With regards to claims 7, 14, and 20, Ross teaches a multiplexer shifts signals on an I/O line to an adjacent multiplexer (output of every multiplexer can be provided back to another multiplexer through its connected device before or after processing, column 17, line 40, through column 18, line 3).

Claim Rejections - 35 USC § 103

22. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

23. Claims 3, 10, and 17, are rejected under 35 U.S.C. 103(a) as being unpatentable over U.S. Patent 5,909,594 to Ross et al. in further view of Logic and Computer Design Fundamentals by Mano and Kime.

24. With regards to claims 3, 10, and 17, Ross does not teach the use of at least one 2-to-1 multiplexer. However, one of ordinary skill in the art at the time of invention would have known that higher order multiplexers are built of lower order multiplexers. Mano and Kime show a 4-1 multiplexer built out of cascaded 2-1 multiplexers (pages 119-120, Fig. 3-20). It would have been obvious to one of ordinary skill in the art at the time of invention to use 2-1 multiplexers for building the higher order multiplexers of Ross, in order to build low complexity higher order multiplexers.

25. With regards to claim 18, Ross teaches at least one multiplexer is a 3-to-1 multiplexer (Fig. 12, elements 611-614).

Conclusion

26. The prior art made of record and not relied upon is considered pertinent to applicant's disclosure. U.S. Patent 5,680,641 to Sidman teaches the use of a plurality of multiplexer and demultiplexers.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Joshua D. Schneider whose telephone number is (571) 272-4158. The examiner can normally be reached on M-F, 8-4:30.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Kim Huynh can be reached on (571) 272-4147. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

JDS

KIM HUYNH
SUPERVISORY PATENT EXAMINER
2/07/06